Full Power Domain SLCR (FPD_SLCR)

Module Name	Full Power Domain SLCR (FPD_SLCR)
Base Address	0xFD610000 FPD_SLCR
Description	Global system level control registers for the full power domain
Vendor Info	Xilinx Inc.

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
wprot0	0x00000000	1	rw	0x00000001	FP Domain SLCR Write protection register
ctrl	0x00000004	1	rw	0x00000000	General control register for the FP Domain SLCR
isr	0x00000008	1	wtc	0x00000000	Interrupt Status Register
imr	0x0000000C	1	ro	0x00000001	Interrupt Mask Register
ier	0x00000010	1	wo	0x00000000	Interrupt Enable Register
idr	0x00000014	1	wo	0x00000000	Interrupt Disable Register
itr	0x00000018	1	wo	0x00000000	Interrupt Trigger Register
WDT_CLK_SEL	0x00000100	32	mixed	0x00000000	SWDT clock source select
INT_FPD	0x00000200	32	mixed	0x00000000	Interconnect Clock Source Select
XPD_REG0	0x00000600	32	rw	0x00000000	Path Delay Block Pre-Load Value
XPD_REG1	0x00000604	32	rw	0x00000000	Path Delay Block Expected Value
XPD_CTRL0	0x00000608	32	mixed	0x00000000	Path Delay Control Register 0
XPD_CTRL1	0x0000060C	32	mixed	0x00000000	Path Delay Control Register 1
XPD_CTRL2	0x00000614	32	mixed	0x00000000	Path Delay Control Register 2
XPD_CTRL3	0x00000618	32	mixed	0x00000000	Path Delay Control Register 3
XPD_SOFT_RST	0x0000061C	32	mixed	0x00000000	Path Delay Sfotware reset register
XPD_STAT	0x00000620	32	mixed	0x00000000	Path Delay Status
eco	0x00000FFC	32	rw	0x00000000	reserved for eco
gpu_reg0	0x00001000	32	rw	0x000046CB	GPU Control Register
gpu_reg1	0x00001004	32	rw	0x000046CB	GPU Control Register
gpu_reg2	0x00001008	32	rw	0x046CB6CB	GPU Control Register
gpu	0x0000100C	32	mixed	0x00000007	GPU Idle status Register
gpu_reg3	0x00001010	32	rw	0x0020B2CB	GPU Control Register
gdma_cfg	0x00003000	7	ro	0x00000048	GDMA RF2 Configuation
GDMA_RAM	0x00003010	16	mixed	0x00003B3B	RAM control register
afi_fs	0x00005000	32	mixed	0x00000A00	afi fs SLCR control register. This register is static and should not be modified during operation.
ERR_ATB_ISR	0x00006000	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
ERR_ATB_IMR	0x00006004	32	ro	0x00000007	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
ERR_ATB_IER	0x00006008	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
ERR_ATB_IDR	0x0000600C	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
ATB_CMD_STORE_EN	0x00006010	32	rw	0x00000007	ATB Sideband Signals
ATB_RESP_EN	0x00006014	32	rw	0x00000000	ATB Sideband Signals
ATB_RESP_TYPE	0x00006018	32	rw	0x00000007	Register to specify the type of response generated by the AXI

					Timeout Block
ATB_PRESCALE	0x00006020	32	rw	0x0000FFFF	ATB Sideband Signals

Secure Full Power Domain SLCR (FPD_SLCR_SECURE)

Module Name	Secure Full Power Domain SLCR (FPD_SLCR_SECURE)
Base Address	0xFD690000 FPD_SLCR_SECURE
Description	Global secure system level control registers
Vendor Info	Xilinx Inc.

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
wprot0	0x00000000	1	rw	0x00000001	LP Domain SLCR Write protection register (Not in use)
ctrl	0x00000004	1	rw	0x00000000	General control register for the LP SLCR
isr	0x00000008	1	wtc	0x00000000	Interrupt Status Register
imr	0x0000000C	1	ro	0x00000001	Interrupt Mask Register
ier	0x00000010	1	wo	0x00000000	Interrupt Enable Register
idr	0x00000014	1	wo	0x00000000	Interrupt Disable Register
itr	0x00000018	1	wo	0x00000000	Interrupt Trigger Register
eco	0x0000001C	32	rw	0x00000000	reserved for eco
slcr_sata	0x00000020	32	rw	0x0000000E	SATA TrustZone settings. This register may only be modified during bootup (while SATA block is disabled)
slcr_pcie	0x00000030	32	rw	0x01FFFFFF	PCIe TrustZone settings. This register may only be modified during bootup (while PCIe block is disabled)
slcr_dpdma	0x00000040	32	rw	0x00000001	DPDMA TrustZone Settings
slcr_gdma	0x00000050	8	rw	0x000000FF	GDMA Trustzone Settings
slcr_gic	0x00000060	1	rw	0x00000000	GIC settings

iou slcr regsiters (IOU_SLCR)

Module Name	iou slcr regsiters (IOU_SLCR)
Base Address	0xFF180000 IOU_SLCR
Description	Global system level control registers for the iou
Vendor Info	Xilinx Inc.

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
MIO_PIN_0	0x00000000	32	rw	0x00000000	Configures MIO Pin 0 peripheral interface mapping. S
MIO_PIN_1	0x00000004	32	rw	0x00000000	Configures MIO Pin 1 peripheral interface mapping
MIO_PIN_2	0x00000008	32	rw	0x00000000	Configures MIO Pin 2 peripheral interface mapping
MIO_PIN_3	0x0000000C	32	rw	0x00000000	Configures MIO Pin 3 peripheral interface mapping
MIO_PIN_4	0x00000010	32	rw	0x00000000	Configures MIO Pin 4 peripheral interface mapping
MIO_PIN_5	0x00000014	32	rw	0x00000000	Configures MIO Pin 5 peripheral interface mapping
MIO_PIN_6	0x00000018	32	rw	0x00000000	Configures MIO Pin 6 peripheral interface mapping
MIO_PIN_7	0x0000001C	32	rw	0x00000000	Configures MIO Pin 7 peripheral interface mapping
MIO_PIN_8	0x00000020	32	rw	0x00000000	Configures MIO Pin 8 peripheral interface mapping
MIO_PIN_9	0x00000024	32	rw	0x00000000	Configures MIO Pin 9 peripheral interface mapping
MIO_PIN_10	0x00000028	32	rw	0x00000000	Configures MIO Pin 10 peripheral interface mapping
MIO_PIN_11	0x0000002C	32	rw	0x00000000	Configures MIO Pin 11 peripheral interface mapping
MIO_PIN_12	0x00000030	32	rw	0x00000000	Configures MIO Pin 12 peripheral interface mapping
MIO_PIN_13	0x00000034	32	rw	0x00000000	Configures MIO Pin 13 peripheral interface mapping
MIO_PIN_14	0x00000038	32	rw	0x00000000	Configures MIO Pin 14 peripheral interface mapping
MIO_PIN_15	0x0000003C	32	rw	0x00000000	Configures MIO Pin 15 peripheral interface mapping
MIO_PIN_16	0x00000040	32	rw	0x00000000	Configures MIO Pin 16 peripheral interface mapping
MIO_PIN_17	0x00000044	32	rw	0x00000000	Configures MIO Pin 17 peripheral interface mapping
MIO_PIN_18	0x00000048	32	rw	0x00000000	Configures MIO Pin 18 peripheral interface mapping
MIO_PIN_19	0x0000004C	32	rw	0x00000000	Configures MIO Pin 19 peripheral interface mapping
MIO_PIN_20	0x00000050	32	rw	0x00000000	Configures MIO Pin 20 peripheral interface mapping
MIO_PIN_21	0x00000054	32	rw	0x00000000	Configures MIO Pin 21 peripheral interface mapping
MIO_PIN_22	0x00000058	32	rw	0x00000000	Configures MIO Pin 22 peripheral interface mapping
MIO_PIN_23	0x0000005C	32	rw	0x00000000	Configures MIO Pin 23 peripheral interface mapping
MIO_PIN_24	0x00000060	32	rw	0x00000000	Configures MIO Pin 24 peripheral interface mapping
MIO_PIN_25	0x00000064	32	rw	0x00000000	Configures MIO Pin 25 peripheral

					interface mapping
MIO_PIN_26	0x00000068	32	rw	0x00000000	Configures MIO Pin 26 peripheral interface mapping
MIO_PIN_27	0x0000006C	32	rw	0x00000000	Configures MIO Pin 27 peripheral interface mapping
MIO_PIN_28	0x00000070	32	rw	0x00000000	Configures MIO Pin 28 peripheral interface mapping
MIO_PIN_29	0x00000074	32	rw	0x00000000	Configures MIO Pin 29 peripheral interface mapping
MIO_PIN_30	0x00000078	32	rw	0x00000000	Configures MIO Pin 30 peripheral interface mapping
MIO_PIN_31	0x0000007C	32	rw	0x00000000	Configures MIO Pin 31 peripheral interface mapping
MIO_PIN_32	0x00000080	32	rw	0x00000000	Configures MIO Pin 32 peripheral interface mapping
MIO_PIN_33	0x00000084	32	rw	0x00000000	Configures MIO Pin 33 peripheral interface mapping
MIO_PIN_34	0x00000088	32	rw	0x00000000	Configures MIO Pin 34 peripheral interface mapping
MIO_PIN_35	0x0000008C	32	rw	0x00000000	Configures MIO Pin 35 peripheral interface mapping
MIO_PIN_36	0x00000090	32	rw	0x00000000	Configures MIO Pin 36 peripheral interface mapping
MIO_PIN_37	0x00000094	32	rw	0x00000000	Configures MIO Pin 37 peripheral interface mapping
MIO_PIN_38	0x00000098	32	rw	0x00000000	Configures MIO Pin 38 peripheral interface mapping
MIO_PIN_39	0x0000009C	32	rw	0x00000000	Configures MIO Pin 39 peripheral interface mapping
MIO_PIN_40	0x000000A0	32	rw	0x00000000	Configures MIO Pin 40 peripheral interface mapping
MIO_PIN_41	0x000000A4	32	rw	0x00000000	Configures MIO Pin 41 peripheral interface mapping
MIO_PIN_42	0x000000A8	32	rw	0x00000000	Configures MIO Pin 42 peripheral interface mapping
MIO_PIN_43	0x000000AC	32	rw	0x00000000	Configures MIO Pin 43 peripheral interface mapping
MIO_PIN_44	0x000000B0	32	rw	0x00000000	Configures MIO Pin 44 peripheral interface mapping
MIO_PIN_45	0x000000B4	32	rw	0x00000000	Configures MIO Pin 45 peripheral interface mapping
MIO_PIN_46	0x000000B8	32	rw	0x00000000	Configures MIO Pin 46 peripheral interface mapping
MIO_PIN_47	0x000000BC	32	rw	0x00000000	Configures MIO Pin 47 peripheral interface mapping
MIO_PIN_48	0x000000C0	32	rw	0x00000000	Configures MIO Pin 48 peripheral interface mapping
MIO_PIN_49	0x000000C4	32	rw	0x00000000	Configures MIO Pin 49 peripheral interface mapping
MIO_PIN_50	0x000000C8	32	rw	0x00000000	Configures MIO Pin 50 peripheral interface mapping
MIO_PIN_51	0x000000CC	32	rw	0x00000000	Configures MIO Pin 51 peripheral interface mapping
MIO_PIN_52	0x000000D0	32	rw	0x00000000	Configures MIO Pin 52 peripheral interface mapping
MIO_PIN_53	0x000000D4	32	rw	0x00000000	Configures MIO Pin 53 peripheral interface mapping
MIO_PIN_54	0x000000D8	32	rw	0x00000000	Configures MIO Pin 54 peripheral interface mapping
MIO_PIN_55	0x000000DC	32	rw	0x00000000	Configures MIO Pin 55 peripheral interface mapping

MIO_PIN_56	0x000000E0	32	rw	0x00000000	Configures MIO Pin 56 peripheral interface mapping
MIO_PIN_57	0x000000E4	32	rw	0x00000000	Configures MIO Pin 57 peripheral interface mapping
MIO_PIN_58	0x000000E8	32	rw	0x00000000	Configures MIO Pin 58 peripheral interface mapping
MIO_PIN_59	0x000000EC	32	rw	0x00000000	Configures MIO Pin 59 peripheral interface mapping
MIO_PIN_60	0x000000F0	32	rw	0x00000000	Configures MIO Pin 60 peripheral interface mapping
MIO_PIN_61	0x000000F4	32	rw	0x00000000	Configures MIO Pin 61 peripheral interface mapping
MIO_PIN_62	0x000000F8	32	rw	0x00000000	Configures MIO Pin 62 peripheral interface mapping
MIO_PIN_63	0x000000FC	32	rw	0x00000000	Configures MIO Pin 63 peripheral interface mapping
MIO_PIN_64	0x00000100	32	rw	0x00000000	Configures MIO Pin 64 peripheral interface mapping
MIO_PIN_65	0x00000104	32	rw	0x00000000	Configures MIO Pin 65 peripheral interface mapping
MIO_PIN_66	0x00000108	32	rw	0x00000000	Configures MIO Pin 66 peripheral interface mapping
MIO_PIN_67	0x0000010C	32	rw	0x00000000	Configures MIO Pin 67 peripheral interface mapping
MIO_PIN_68	0x00000110	32	rw	0x00000000	Configures MIO Pin 68 peripheral interface mapping
MIO_PIN_69	0x00000114	32	rw	0x00000000	Configures MIO Pin 69 peripheral interface mapping
MIO_PIN_70	0x00000118	32	rw	0x00000000	Configures MIO Pin 70 peripheral interface mapping
MIO_PIN_71	0x0000011C	32	rw	0x00000000	Configures MIO Pin 71 peripheral interface mapping
MIO_PIN_72	0x00000120	32	rw	0x00000000	Configures MIO Pin 72 peripheral interface mapping
MIO_PIN_73	0x00000124	32	rw	0x00000000	Configures MIO Pin 73 peripheral interface mapping
MIO_PIN_74	0x00000128	32	rw	0x00000000	Configures MIO Pin 74 peripheral interface mapping
MIO_PIN_75	0x0000012C	32	rw	0x00000000	Configures MIO Pin 75 peripheral interface mapping
MIO_PIN_76	0x00000130	32	rw	0x00000000	Configures MIO Pin 76 peripheral interface mapping
MIO_PIN_77	0x00000134	32	rw	0x00000000	Configures MIO Pin 77 peripheral interface mapping
bank0_ctrl0	0x00000138	26	rw	0x03FFFFFF	Drive0 control to MIO Bank 0 - control MIO[25:0]
bank0_ctrl1	0x0000013C	26	rw	0x00000000	Drive1 control to MIO Bank 0 - control MIO[25:0]
bank0_ctrl3	0x00000140	26	rw	0x00000000	Selects either Schmitt or CMOS input for MIO Bank 0 - control MIO[25:0]
bank0_ctrl4	0x00000144	26	rw	0x03FFFFFF	When mio_bank0_pull_enable is set, this selects pull up or pull down for MIO Bank 0 - control MIO[25:0]
bank0_ctrl5	0x00000148	26	rw	0x03FFFFFF	When set, this enables mio_bank0_pullupdown to selects pull up or pull down for MIO Bank 0 - control MIO[25:0]
bank0_ctrl6	0x0000014C	26	rw	0x00000000	Slew rate control to MIO Bank 0 - control MIO[25:0]
bank0_status	0x00000150	1	ro	x	voltage mode status of the IO bank

bank1_ctrl0	0x00000154	26	rw	0x03FFFFFF	Drive0 control to MIO Bank 1 - control MIO[51:26]
bank1_ctrl1	0x00000158	26	rw	0x00000000	Drive1 control to MIO Bank 1 - control MIO[51:26]
bank1_ctrl3	0x0000015C	26	rw	0x00000000	Selects either Schmitt or CMOS input for MIO Bank 1 - control MIO[51:26]
bank1_ctrl4	0x00000160	26	rw	0x03FFFFFF	When mio_bank1_pull_enable is set, this selects pull up or pull down for MIO Bank 1 - control MIO[51:26]
bank1_ctrl5	0x00000164	26	rw	0x03FFFFFF	When set, this enables mio_bank1_pullupdown to selects pull up or pull down for MIO Bank 1 - control MIO[51:26]
bank1_ctrl6	0x00000168	26	rw	0x00000000	Slew rate control to MIO Bank 1 - control MIO[51:26]
bank1_status	0x0000016C	1	ro	x	voltage mode status of the IO bank
bank2_ctrl0	0x00000170	26	rw	0x03FFFFFF	Drive0 control to MIO Bank 2 - control MIO[77:52]
bank2_ctrl1	0x00000174	26	rw	0x00000000	Drive1 control to MIO Bank 2 - control MIO[77:52]
bank2_ctrl3	0x00000178	26	rw	0x00000000	Selects either Schmitt or CMOS input for MIO Bank 2 - control MIO[77:52]
bank2_ctrl4	0x0000017C	26	rw	0x03FFFFFF	When mio_bank2_pull_enable is set, this selects pull up or pull down for MIO Bank 2 - control MIO[77:52]
bank2_ctrl5	0x00000180	26	rw	0x03FFFFFF	When set, this enables mio_bank2_pullupdown to selects pull up or pull down for MIO Bank 2 - control MIO[77:52]
bank2_ctrl6	0x00000184	26	rw	0x00000000	Slew rate control to MIO Bank 2 - control MIO[77:52]
bank2_status	0x00000188	1	ro	x	voltage mode status of the IO bank
MIO_LOOPBACK	0x00000200	32	mixed	0x00000000	Loopback function within MIO
MIO_MST_TRI0	0x00000204	32	rw	0xFFFFFFFF	MIO pin Tri-state Enables, 31:0
MIO_MST_TRI1	0x00000208	32	rw	0xFFFFFFFF	MIO pin Tri-state Enables, 63:32
MIO_MST_TRI2	0x0000020C	32	mixed	0x00003FFF	MIO pin Tri-state Enables, 77:64
WDT_CLK_SEL	0x00000300	32	mixed	0x00000000	SWDT clock source select
CAN_MIO_CTRL	0x00000304	32	mixed	0x00000000	CAN MIO Control
GEM_CLK_CTRL	0x00000308	32	mixed	0x00000000	SoC Debug Clock Control
SDIO_CLK_CTRL	0x0000030C	32	mixed	0x00000000	SoC Debug Clock Control
CTRL_REG_SD	0x00000310	32	mixed	0x00000000	SD eMMC selection
SD_ITAPDLY	0x00000314	32	mixed	0x00000000	Input Tap Delay Select
SD_OTAPDLYSEL	0x00000318	32	mixed	0x00000000	Output Tap Delay Select (0 to 15)
SD_CONFIG_REG1	0x0000031C	32	mixed	0x32403240	SD Config Register 1
SD_CONFIG_REG2	0x00000320	32	mixed	0x0FFC0FFC	SD Config Register 2
SD_CONFIG_REG3	0x00000324	32	mixed	0x06070607	SD Config Register 3
SD_INITPRESET	0x00000328	32	mixed	0x01000100	Preset Value for Initialization
SD_DSPPRESET	0x0000032C	32	mixed	0x00040004	Preset Value for Default Speed
SD_HSPDPRESET	0x00000330	32	mixed	0x00020002	Preset Value for High Speed
SD_SDR12PRESET	0x00000334	32	mixed	0x00040004	Preset Value for SDR12
SD_SDR25PRESET	0x00000338	32	mixed	0x00020002	Preset Value for SDR25
SD_SDR50PRSET	0x0000033C	32	mixed	0x00010001	Preset Value for SDR50
SD_SDR104PRST	0x00000340	32	mixed	0x00000000	Preset Value for SDR104
SD_DDR50PRESET	0x00000344	32	mixed	0x00020002	Preset Value for DDR50
SD_MAXCUR1P8	0x0000034C	32	mixed	0x00000000	Maximum Current for 1.8V
SD_MAXCUR3P0	0x00000350	32	mixed	0x00000000	Maximum Current for 3.0V
SD_MAXCUR3P3	0x00000354	32	mixed	0x00000000	Maximum Current for 3.3V

SD_DLL_CTRL	0x00000358	32	mixed	x	SDIO status register
SD_CDn_CTRL	0x0000035C	32	mixed	0x00000000	SDIO CDn control register
GEM_CTRL	0x00000360	32	mixed	0x00000000	GEM SGMII Signal Detect control register
IOU_TTC_APB_CLK	0x00000380	32	mixed	0x00000000	TTC APB clock select
IOU_TAPDLY_BYPASS	0x00000390	32	mixed	0x00000007	IOU tap delay bypass for the LQSPI and NAND controllers
IOU_COHERENT_CTRL	0x00000400	32	rw	0x00000000	AXI Coherency selection
VIDEO_PSS_CLK_SEL	0x00000404	32	mixed	0x00000000	VIDEO_CLK and PSS_ALT_REF_CLK selection from MIO pins
IOU_INTERCONNECT_ROUTE	0x00000408	32	mixed	0x00000000	Route the IOU DMA master transaction to CCI
IOU_RAM_GEM0	0x00000500	32	mixed	0x00005B5B	GEM0 RX/TX RAM controls (four RAMs)
IOU_RAM_GEM1	0x00000504	32	mixed	0x00005B5B	GEM1 RX/TX RAM controls (four RAMs)
IOU_RAM_GEM2	0x00000508	32	mixed	0x00005B5B	GEM2 RX/TX RAM controls (four RAMs)
IOU_RAM_GEM3	0x0000050C	32	mixed	0x00005B5B	GEM3 RX/TX RAM controls (four RAMs)
IOU_RAM_SD0	0x00000510	32	mixed	0x0000005B	SDIO 0 RAM controls
IOU_RAM_SD1	0x00000514	32	mixed	0x0000005B	SDIO 1 RAM controls
IOU_RAM_CAN0	0x00000518	32	mixed	0x005B5B5B	CAN 0 RAM controls (four RAMs)
IOU_RAM_CAN1	0x0000051C	32	mixed	0x005B5B5B	CAN 1 RAM controls (three RAMs)
IOU_RAM_LQSPI	0x00000520	32	mixed	0x00002DDB	Quad SPI RAM controls (two RAMs)
IOU_RAM_NAND	0x00000524	32	mixed	0x0000005B	NAND RAM controls (1 RAM)
ctrl	0x00000600	1	rw	0x00000000	General control register for the IOU SLCR
isr	0x00000700	1	wtc	0x00000000	Interrupt Status Register
imr	0x00000704	1	ro	0x00000001	Interrupt Mask Register
ier	0x00000708	1	wo	0x00000000	Interrupt Enable Register
idr	0x0000070C	1	wo	0x00000000	Interrupt Disable Register
itr	0x00000710	1	wo	0x00000000	Interrupt Trigger Register
eco	0x00000730	32	rw	0x00000000	reserved for eco
XPD_REG0	0x00000800	32	rw	0x00000000	Path Delay Block Pre-Load Value
XPD_REG1	0x00000804	32	rw	0x00000000	Path Delay Block Expected Value
XPD_CTRL0	0x00000808	32	mixed	0x00000000	Path Delay Control Register 0
XPD_CTRL1	0x0000080C	32	mixed	0x00000000	Path Delay Control Register 1
XPD_CTRL2	0x00000814	32	mixed	0x00000000	Path Delay Control Register 2
XPD_CTRL3	0x00000818	32	mixed	0x00000000	Path Delay Control Register 3
XPD_SOFT_RST	0x0000081C	32	mixed	0x00000000	Path Delay Sfotware reset register
XPD_STAT	0x00000820	32	mixed	0x00000000	Path Delay Status

iou secure slcr regsiters (IOU_SECURE_SLCR)

Module Name	iou secure slcr regsiters (IOU_SECURE_SLCR)
Base Address	0xFF240000 IOU_SECURE_SLCR
Description	Global system level control registers for the iou
Vendor Info	Xilinx Inc.

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
IOU_AXI_WPRTCN	0x00000000	32	mixed	0x00000000	AXI write protection type selection
IOU_AXI_RPRTCN	0x00000004	32	mixed	0x00000000	AXI read protection type selection
ctrl	0x00000040	1	rw	0x00000000	General control register for the IOU SLCR
isr	0x00000044	1	wtc	0x00000000	Interrupt Status Register
imr	0x00000048	1	ro	0x00000001	Interrupt Mask Register
ier	0x0000004C	1	wo	0x00000000	Interrupt Enable Register
idr	0x00000050	1	wo	0x00000000	Interrupt Disable Register
itr	0x00000054	1	wo	0x00000000	Interrupt Trigger Register
eco	0x00000080	32	rw	0x00000000	reserved for eco

Low Power Domain SLCR (LPD_SLCR)

Module Name	Low Power Domain SLCR (LPD_SLCR)
Base Address	0xFF410000 LPD_SLCR
Description	Global system level control registers for the low power domain
Vendor Info	Xilinx Inc.

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
wprot0	0x00000000	1	rw	0x00000001	LP Domain SLCR Write protection register
ctrl	0x00000004	1	rw	0x00000000	General control register for the LP SLCR
isr	0x00000008	1	wtc	0x00000000	Interrupt Status Register
imr	0x0000000C	1	ro	0x00000001	Interrupt Mask Register
ier	0x00000010	1	wo	0x00000000	Interrupt Enable Register
idr	0x00000014	1	wo	0x00000000	Interrupt Disable Register
itr	0x00000018	1	wo	0x00000000	Interrupt Trigger Register
eco	0x0000001C	32	rw	0x00000000	reserved for eco
persistent0	0x00000020	32	rw	x	This register is never reset, even through POR.
persistent1	0x00000024	32	rw	x	This register is never reset, even through POR.
persistent2	0x00000028	32	rw	x	This register is never reset, even through POR.
persistent3	0x0000002C	32	rw	x	This register is never reset, even through POR.
persistent4	0x00000030	32	rw	x	This register is never reset, even through POR.
persistent5	0x00000034	32	rw	x	This register is never reset, even through POR.
persistent6	0x00000038	32	rw	x	This register is never reset, even through POR.
persistent7	0x0000003C	32	rw	x	This register is never reset, even through POR.
SAFETY_CHK0	0x00000040	32	rw	0x00000000	Safety endpoint connectivity check Register
SAFETY_CHK1	0x00000044	32	rw	0x00000000	Safety endpoint connectivity check Register
SAFETY_CHK2	0x00000048	32	rw	0x00000000	Safety endpoint connectivity check Register
SAFETY_CHK3	0x0000004C	32	rw	0x00000000	Safety endpoint connectivity check Register
CSUPMU_WDT_CLK_SEL	0x00000050	32	mixed	0x00000000	SWDT clock source select
adma_cfg	0x0000200C	7	ro	0x00000028	GDMA RF2 Configuation
ADMA_RAM	0x00002010	16	mixed	0x00003B3B	RAM control register
ERR_AIBAXI_ISR	0x00003000	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
ERR_AIBAXI_IMR	0x00003008	32	ro	0x1DCF000F	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
ERR_AIBAXI_IER	0x00003010	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
ERR_AIBAXI_IDR	0x00003018	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the

					interrupt. (IMR: 1)
ERR_AIBAPB_ISR	0x00003020	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
ERR_AIBAPB_IMR	0x00003024	32	ro	0x00000001	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
ERR_AIBAPB_IER	0x00003028	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
ERR_AIBAPB_IDR	0x0000302C	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
ISO_AIBAXI_REQ	0x00003030	32	rw	0x00000000	Request to AIB to start Isolation. '1' Isolate. '0' No Isolation
ISO_AIBAXI_TYPE	0x00003038	32	rw	0x19CF000F	If '1' AIB sends SLVERR. If '0' AIB does not respond
ISO_AIBAXI_ACK	0x00003040	32	ro	0x00000000	If '1' AIB has Functionally Isolated Master and Slave
ISO_AIBAPB_REQ	0x00003048	32	rw	0x00000000	Request to AIB to start Isolation. '1' Isolate. '0' No Isolation
ISO_AIBAPB_TYPE	0x0000304C	32	rw	0x00000001	If '1' AIB sends SLVERR. If '0' AIB does not respond
ISO_AIBAPB_ACK	0x00003050	32	ro	0x00000000	If '1' AIB has Functionally Isolated Master and Slave
ERR_ATB_ISR	0x00006000	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
ERR_ATB_IMR	0x00006004	32	ro	0x00000003	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
ERR_ATB_IER	0x00006008	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
ERR_ATB_IDR	0x0000600C	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
ATB_CMD_STORE_EN	0x00006010	32	rw	0x00000003	ATB Sideband Signals
ATB_RESP_EN	0x00006014	32	rw	0x00000000	ATB Sideband Signals
ATB_RESP_TYPE	0x00006018	32	rw	0x00000003	ATB Sideband Signals
ATB_ERR_INJECT	0x0000601C	32	rw	0x00000000	ATB Sideband Signals
ATB_PRESCALE	0x00006020	32	rw	0x0000FFFF	ATB Sideband Signals
Mutex0	0x00007000	32	rw	0x00000000	LP Domain SLCR Mutex 0 register
Mutex1	0x00007004	32	rw	0x00000000	LP Domain SLCR Mutex 1 register
Mutex2	0x00007008	32	rw	0x00000000	LP Domain SLCR Mutex 2 register
Mutex3	0x0000700C	32	rw	0x00000000	LP Domain SLCR Mutex 3 register
GICP0_IRQ_STATUS	0x00008000	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP0_IRQ_MASK	0x00008004	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP0_IRQ_ENABLE	0x00008008	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP0_IRQ_DISABLE	0x0000800C	32	wo	0x00000000	Interrupt Disable Register. A write of

					one to this location will mask the interrupt. (IMR: 1)
GICP0_IRQ_TRIGGER	0x00008010	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP1_IRQ_STATUS	0x00008014	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP1_IRQ_MASK	0x00008018	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP1_IRQ_ENABLE	0x0000801C	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP1_IRQ_DISABLE	0x00008020	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP1_IRQ_TRIGGER	0x00008024	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP2_IRQ_STATUS	0x00008028	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP2_IRQ_MASK	0x0000802C	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP2_IRQ_ENABLE	0x00008030	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP2_IRQ_DISABLE	0x00008034	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP2_IRQ_TRIGGER	0x00008038	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP3_IRQ_STATUS	0x0000803C	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP3_IRQ_MASK	0x00008040	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP3_IRQ_ENABLE	0x00008044	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP3_IRQ_DISABLE	0x00008048	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP3_IRQ_TRIGGER	0x0000804C	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP4_IRQ_STATUS	0x00008050	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP4_IRQ_MASK	0x00008054	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN.

					This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP4_IRQ_ENABLE	0x00008058	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP4_IRQ_DISABLE	0x0000805C	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP4_IRQ_TRIGGER	0x00008060	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP5_IRQ_STATUS	0x00008064	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP5_IRQ_MASK	0x00008068	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP5_IRQ_ENABLE	0x0000806C	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP5_IRQ_DISABLE	0x00008070	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP5_IRQ_TRIGGER	0x00008074	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP6_IRQ_STATUS	0x00008078	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP6_IRQ_MASK	0x0000807C	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP6_IRQ_ENABLE	0x00008080	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP6_IRQ_DISABLE	0x00008084	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP6_IRQ_TRIGGER	0x00008088	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
GICP7_IRQ_STATUS	0x0000808C	32	wtc	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP7_IRQ_MASK	0x00008090	32	ro	0xFFFFFFFF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP7_IRQ_ENABLE	0x00008094	32	wo	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP7_IRQ_DISABLE	0x00008098	32	wo	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP7_IRQ_TRIGGER	0x0000809C	32	wo	0x00000000	Interrupt Trigger Register. A write of one to this location will set the

					interrupt status register related to this interrupt.
GICP_PMU_IRQ_STATUS	0x000080A0	32	mixed	0x00000000	Interrupt Status Register for intrN. This is a sticky register that holds the value of the interrupt until cleared by a value of 1.
GICP_PMU_IRQ_MASK	0x000080A4	32	mixed	0x000000FF	Interrupt Mask Register for intrN. This is a read-only location and can be atomically altered by either the IDR or the IER.
GICP_PMU_IRQ_ENABLE	0x000080A8	32	mixed	0x00000000	Interrupt Enable Register. A write of to this location will unmask the interrupt. (IMR: 0)
GICP_PMU_IRQ_DISABLE	0x000080AC	32	mixed	0x00000000	Interrupt Disable Register. A write of one to this location will mask the interrupt. (IMR: 1)
GICP_PMU_IRQ_TRIGGER	0x000080B0	32	mixed	0x00000000	Interrupt Trigger Register. A write of one to this location will set the interrupt status register related to this interrupt.
afi_fs	0x00009000	16	mixed	0x00000200	afi fs SLCR control register. Do not change the bits durin
lpd_cci	0x0000A000	32	rw	0x03801C07	CCI Configuration. This register may be written to only when FPD Interconnect is in reset.
lpd_cci_addrmap	0x0000A004	32	rw	0x00C000FF	Address Decode for each reguion of the address map of CCI. This register may be written to only when FPD Interconnect is in reset.
lpd_cci_qvnprealloc	0x0000A008	32	mixed	0x00330330	QVN Preallocation Configuration
lpd_smmu	0x0000A020	32	rw	0x0000003F	SMMU Configuration. This register may be written to only when FPD Interconnect is in reset.
lpd_apu	0x0000A040	32	rw	0x00000001	APU Configuration. This register may be written to only when APU is in reset

Secure Low Power Domain SLCR (LPD_SLCR_SECURE)

Module Name	Secure Low Power Domain SLCR (LPD_SLCR_SECURE)
Base Address	0xFF4B0000 LPD_SLCR_SECURE
Description	Global secure system level control registers
Vendor Info	Xilinx Inc.

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
wprot0	0x00000000	1	rw	0x00000001	LP Domain SLCR Write protection register (No in use)
ctrl	0x00000004	1	rw	0x00000000	General control register for the LP SLCR
isr	0x00000008	1	wtc	0x00000000	Interrupt Status Register
imr	0x0000000C	1	ro	0x00000001	Interrupt Mask Register
ier	0x00000010	1	wo	0x00000000	Interrupt Enable Register
idr	0x00000014	1	wo	0x00000000	Interrupt Disable Register
itr	0x00000018	1	wo	0x00000000	Interrupt Trigger Register
eco	0x0000001C	32	rw	0x00000000	reserved for eco
slcr_rpu	0x00000020	2	rw	0x00000000	RPU TrustZone settings
slcr_adma	0x00000024	8	rw	0x00000000	RPU TrustZone settings
SAFETY_CHK	0x00000030	32	rw	0x00000000	Safety endpoint connectivity check Register
slcr_usb	0x00000034	2	rw	0x00000003	USB3 TrustZone settings